DESIGNING NON-LINEAR SINGLE OP-AMP CIRCUITS: A COOK-BOOK APPROACH

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SUMMARY

The inherent saturation *non-linearity* of the op amp is used to design circuits having a wide variety of useful non-linear v–i characteristics. These circuits are made of one op amp and 3 or 4 linear resistors which are passive under a rather mild assumption derived from the 3-port paramountcy condition. Explicit design formulae are given for each prototype circuit and numerous examples are given and validated by actual measurements.

1. INTRODUCTION

Operational amplifiers (op amps) have been used almost exclusively as a *linear* element in circuit design.[1–3] Even in *non-linear* circuit applications, such as synthesis of precision non-linear driving-point characteristics[4] the op amp is operated only in the *linear region*, and the circuit's non-linear behaviour is provided by other non-linear elements such as *p-n*-junction diodes. Consequently, the dynamic range of the input signal in most op amp circuits must be restricted to avoid driving the op amp into saturation.

In this paper we will exploit, rather than avoid, the inherent non-linearity of the op amp in designing practical circuits. In particular, we will show that any one-port made of *one* op amp and linear positive resistors (Figure 1(a)) is characterized by one of the ten odd-symmetric driving-point characteristics shown in Figure 1(b), assuming that the op amp has a symmetric saturation characteristic. Moreover, we will show that under a rather mild inequality assumption, any of these v–i characteristics can be realized by the *canonical* circuit shown in Figure 2.

Each v–i characteristic in Figure 1(b) has numerous applications:[5–7] characteristics (i)–(iv) in Figure 1(b) can be used for wave shaping applications; characteristics (v) and (vi) can be used for designing oscillators and multivibrators, whereas characteristics (vii)–(x) can be used for designing flip-flops. Moreover, since these characteristics can be realized with high precision, they can be used as *building blocks* for synthesizing more complicated v–i characteristics. Since the origin in each v–i characteristic in Figure 1(b) can be translated to any other point in the v–i plane by adding one or two batteries, we have an unusually large repertoire of accurate v–i characteristic building blocks made of only op amps, linear positive resistors, and batteries.

Because of its widespread applications, Section 2 is written in a 'cook-book' style for users interested only in building the canonical op amp circuits to have any one the v–i characteristics in Figure 1(b) with *prescribed* breakpoints and slopes. Although the canonical circuit in Figure 2 contains 7 resistors, no more than 4 are needed in each case. Consequently, the simplified circuits in Section 2 are all special cases of the canonical circuit. Explicit formulae for calculating the resistances and battery voltages are given for each simplified canonical circuit. To demonstrate the accuracy of these circuits in realizing a prescribed v–i characteristic, examples with experimentally measured v–i characteristics are given for comparison purposes.

Some practical aspects of the circuits presented in Section 2 are discussed in Section 3.

Section 4 is devoted to the design of several practical circuits using the simplified canonical circuits from Section 2 as building blocks.

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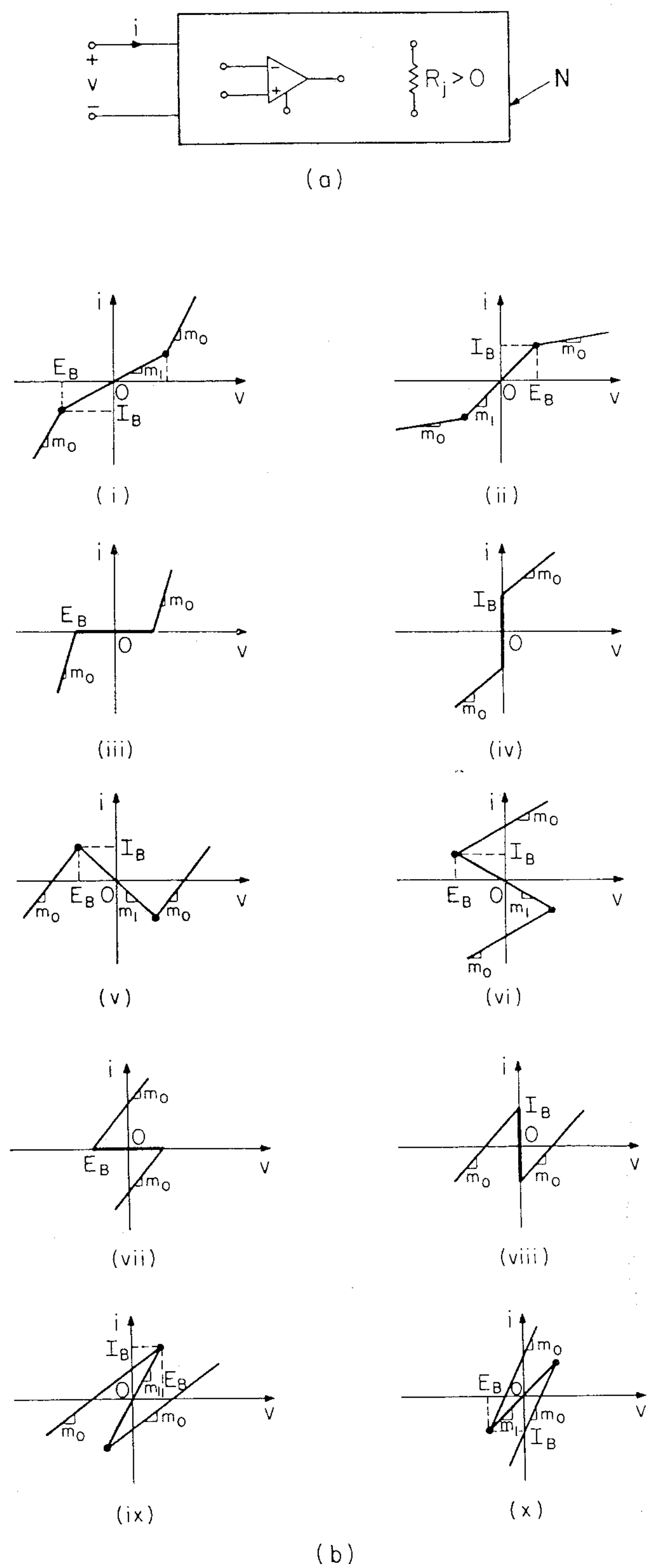


Figure 1. (a) Circuit configuration under study. (b) Possible v–i characteristics for the one-port in (a)

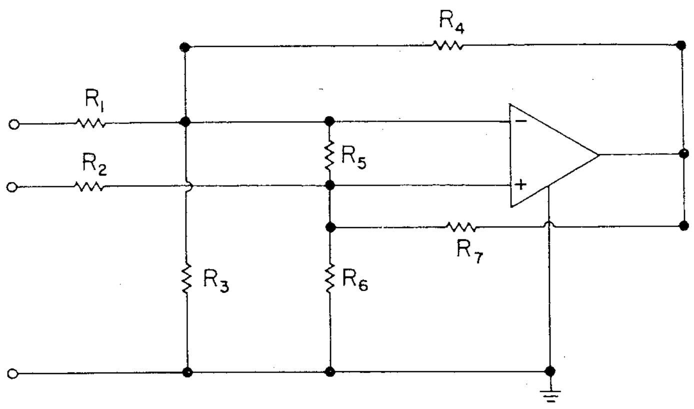


Figure 2. Canonical circuit

The canonical circuit in Figure 2 is derived via a circuit-theoretic approach in Section 5. The concept of a *paramount* matrix[8] plays a crucial role in the conception of this circuit. Indeed, our approach represents one of the very few instances in electronic circuit design where a circuit configuration is derived *systematically* rather than through an *ad hoc* or intuitive approach.

2. DESIGN FORMULAE AND EXAMPLES

Each v–i characteristic in Figure 1 can be synthesized by a simplified version of the canonical circuit in Figure 2. In the following we consider one v–i characteristic at a time (in the order listed) and give the corresponding circuit along with the formulae for calculating the element values. Note that since we retain the resistor label in the canonical circuit, the resistors in the following circuits are not numbered consecutively since only 3 or 4 (out of 7) resistors are needed in each case. Except for E_{s+} and E_{s-} which denote the positive and negative *saturation* voltages of the op amp being used,† all other parameters are labelled in the associated v–i characteristics. In order to guarantee that all resistors are *positive*, it is both *necessary* and *sufficient* that these parameters must satisfy the following standing assumptions:

Slope-breakpoint inequality

$$\left|\frac{m_0 - m_1}{m_0}\right| < \frac{E_{s+} - |E_{s-}|}{E_{B2} - E_{B1}} \tag{1a}$$

$$\frac{E_{B2} - E_{B1}}{E_{s+} + |E_{s-}|} < 1 \tag{1b}$$

for all cases except (iv) and (viii) where (1a) and (1b) are replaced by

$$m_0 > \frac{I_{B2} - I_{B1}}{E_{s+} + |E_{s-}|} \tag{2}$$

The standing assumption will be derived in Section 4. It is a *weak* assumption that is satisfied by most v–i characteristics of practical interest.

Two design examples will be given for each simplified canonical circuit. The first example is an *odd-symmetric* characteristic taken directly from Figure 1. The second example is a *translated* version of the corresponding characteristic from Figure 1. For comparison purposes we have used the *same* op amp

† For improved accuracy in our design we do not assume the op amp saturation voltages to be equal in magnitude. Of course, if an odd-symmetric v–i characteristic is required, then an op amp with $|E_{s+}| = |E_{s-}|$ must be chosen.

(national/8035 741 CN) in all these examples. This op amp was measured to have a positive saturation voltage $E_{s+} = 15$ V and a negative saturation voltage $E_{s-} = -13$ V. Had another op amp with *identical* saturation voltages been chosen, then no batteries would be needed in realizing each odd-symmetric characteristic in the following examples: 1.1, 2.1, 3.1, 4.1, 5.1, 6.1, 7.1, 8.1, 9.1 and 10.1.

v–i characteristic (i)

Consider the v–i characteristic in Figure 3(a). This is identical to the v–i characteristic (i) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 3(b).

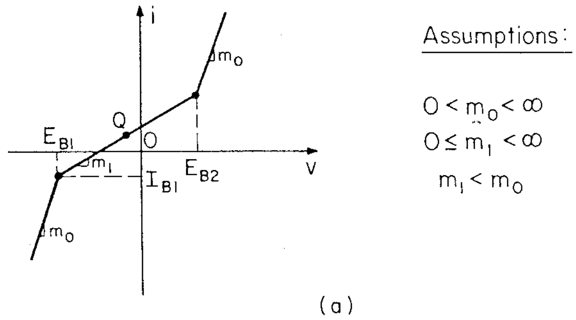
Example 1.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 4(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -1$ V, $E_{B2} = 1$ V and $I_{B1} = -1$ mA. Substituting these parameters into (1), we find

$$\left|\frac{2-1}{1}\right| < \frac{15+13}{1+1} \qquad \left|\frac{1+1}{15+13}\right| < 1$$

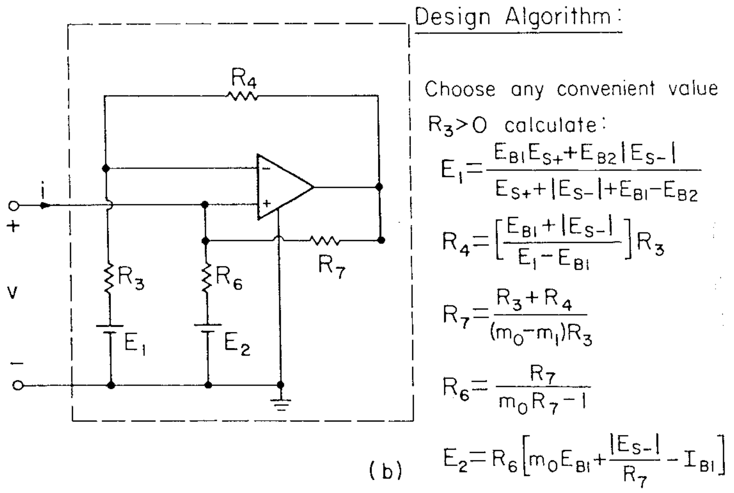
Hence, the slope-breakpoint condition is satisfied and we know that only positive resistors are needed. The element values calculated from the design algorithm in Figure 3(b) are

$$R_3 = 1\ \text{k}\Omega, \quad R_4 = 13\ \text{k}\Omega, \quad R_6 = 518{\cdot}5\ \Omega, \quad R_7 = 14\ \text{k}\Omega, \quad E_1 = -0{\cdot}77\ \text{V}, \quad E_2 = -0{\cdot}37\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 4(b).‡



(a)



(b)

Figure 3. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

† All v–i curves in this paper have been traced with a specially designed negative-resistance curve tracer.[9]

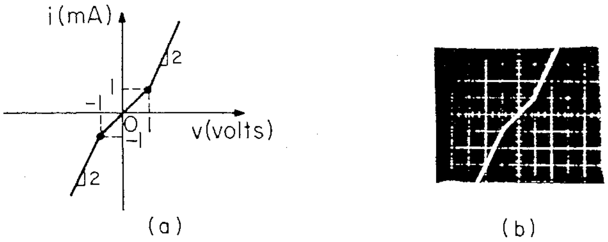


Figure 4. (a) Odd-symmetric characteristic for example 1.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

Example 1.2. Synthesize the v–i characteristic shown in Figure 5(a) using an op amp with $E_{s+}=15$ V and $E_{s-}=-13$ V. Here $m_0=3$, $m_1=1$, $E_{B1}=-3$ V, $E_{B2}=1$ V and $I_{B1}=-2$ mA. The slope-breakpoint condition is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 3(b) are

$$R_3=1\ \text{k}\Omega,\quad R_4=6\ \text{k}\Omega,\quad R_6=368\ \Omega,\quad R_7=3{\cdot}5\ \text{k}\Omega,\quad E_1=-1{\cdot}33\ \text{V},\quad E_2=-1{\cdot}21\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 5(b).

v–i characteristic (ii)

Consider the v–i characteristic in Figure 6(a). This is identical to the v–i characteristic (ii) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 6(b).

Example 2.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 7(a) using an op amp with $E_{s+}=15$ V and $E_{s-}=-13$ V. Here $m_0=1$, $m_1=2$, $E_{B1}=-2$ V, $E_{B2}=2$ V and $I_{B1}=-4$ mA. It is easily verified that condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 6(b) are

$$R_1=500\ \Omega,\quad R_3=583\ \Omega,\quad R_4=3{\cdot}5\ \text{k}\Omega,\quad E_1=-0{\cdot}17\ \text{V},\quad E_2=0$$

The v–i characteristic measured from the resulting circuit is shown in Figure 7(b).

Example 2.2. Synthesize the v–i characteristic shown in Figure 8(a) using an op amp with $E_{s+}=15$ V and $E_{s-}=-13$ V. Here $m_0=1$, $m_1=2$, $E_{B1}=-2$ V, $E_{B2}=4$ V and $I_{B1}=1$ mA. Since condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Figure 6(b) are

$$R_1=500\ \Omega,\quad R_3=633\ \Omega,\quad R_4=2{\cdot}33\ \text{k}\Omega,\quad E_1=-7{\cdot}91\ \text{V},\quad E_2=-2{\cdot}5\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 8(b).

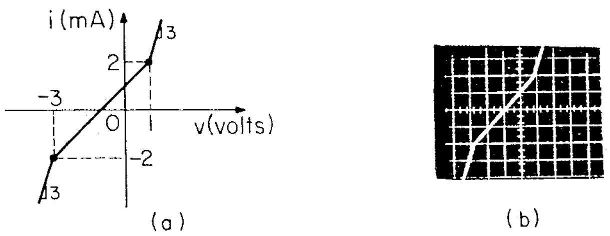


Figure 5. (a) v–i characteristic for example 1.2. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

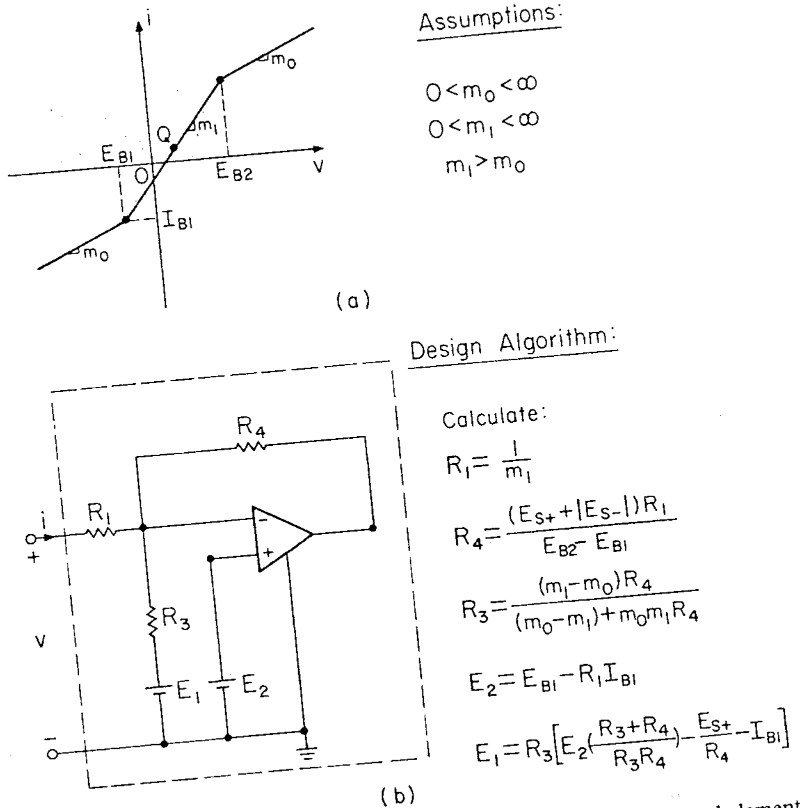


Figure 6. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

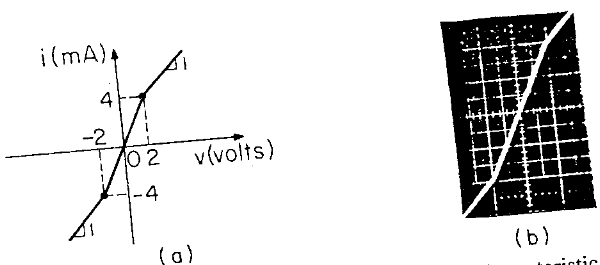


Figure 7. (a) Odd-symmetric characteristic for example 2.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

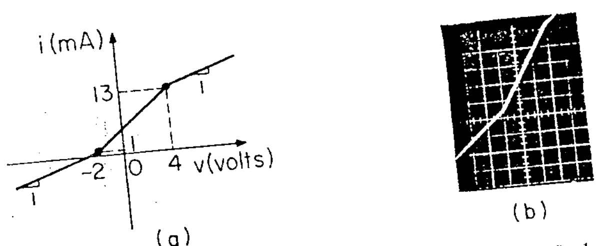
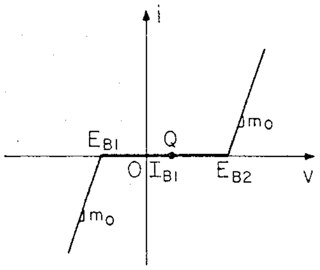


Figure 8. (a) v–i characteristic for example 2.2. (b) Measured v–i characteristic. Scale, i: 5 mA/div, v: 4 V/div

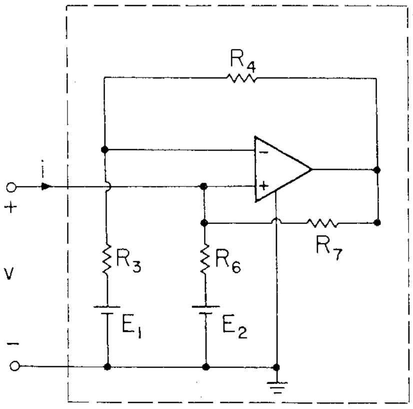


Assumptions:

$0 < m_0 < \infty$

$m_1 = 0$

(a)



Design Algorithm:

Choose any convenient value $R_3 > 0$, calculate:

$$E_1 = \frac{E_{B1}E_{S+} + E_{B2}|E_{S-}|}{E_{S+} + |E_{S-}| + E_{B1} - E_{B2}}$$

$$R_4 = \left[\frac{E_{B1} + |E_{S-}|}{E_1 - E_{B1}}\right] R_3$$

$$R_7 = \frac{R_3 + R_4}{m_0 R_3}$$

$$R_6 = \frac{R_7}{m_0 R_7 - 1}$$

$$E_2 = R_6\left[m_0 E_{B1} + \frac{|E_{S-}|}{R_7} - I_{B1}\right]$$

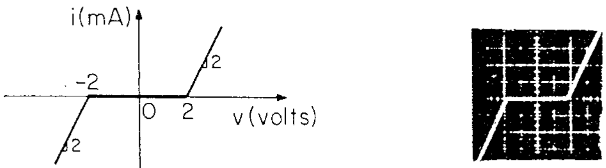
(b)

Figure 9. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

v–i characteristic (iii)

Consider the v–i characteristic in Figure 9(a). This is identical to the v–i characteristic (iii) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 9(b).

Example 3.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 10(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = 0$. Condition (1) is satisfied and only positive resistors are needed. The element values calculated from the



(a) (b)

Figure 10. (a) Odd-symmetric characteristic for example 3.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

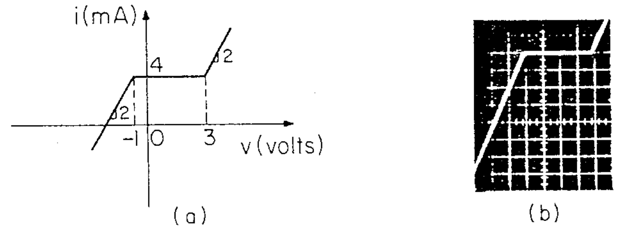


Figure 11. (a) v–i characteristic for example 3.2. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

design algorithm in Figure 9(b) are

$$R_3 = 1\ \text{k}\Omega, \qquad R_4 = 6\ \text{k}\Omega, \qquad R_6 = 583\ \Omega$$

$$R_7 = 3{\cdot}5\ \text{k}\Omega, \qquad E_1 = -0{\cdot}17\ \text{mV}, \qquad E_2 = -0{\cdot}17\ \text{mV}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 10(b).

Example 3.2. Synthesize the v–i characteristic shown in Figure 11(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 0$, $E_{B1} = -1$ V, $E_{B2} = 3$ V and $I_{B1} = 4$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 9(b) are

$$R_3 = 1\ \text{k}\Omega, \qquad R_4 = 6\ \text{k}\Omega, \qquad R_6 = 583\ \Omega, \qquad R_7 = 3{\cdot}5\ \text{k}\Omega, \qquad E_1 = 1\ \text{V}, \qquad E_2 = -1{\cdot}33\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 11(b).

v–i characteristic (iv)

Consider the v–i characteristic in Figure 12(a). This is identical to the v–i characteristic (iv) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 12(b).

Example 4.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 13(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = \frac{1}{4}$, $m_1 = \infty$, $I_{B1} = -3$ mA, $I_{B2} = 3$ mA and $E_{B1} = 0$. Substituting these parameters into (2), we find

$$\frac{1}{4} > \frac{3+3}{15+13}$$

Hence, the slope-breakpoint inequality is satisfied and we know that only positive resistors are needed. The element values calculated from the design algorithm in Figure 12(b) are

$$R_4 = 4{\cdot}7\ \text{k}\Omega, \qquad R_5 = 18\ \text{k}\Omega, \qquad R_6 = 10\ \text{k}\Omega, \qquad E_2 = 0, \qquad E_3 = +1\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 13(b).

Example 4.2. Synthesize the v–i characteristic shown in Figure 14(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = \frac{1}{4}$, $m_1 = \infty$, $I_{B1} = -1$ mA, $I_{B2} = 3$ mA and $E_{B1} = 4$ V. The slope-breakpoint condition (2) is satisfied. The element values calculated from the design algorithm in Figure 12(b) are

$$R_4 = 7\ \text{k}\Omega, \qquad R_5 = 1\ \text{k}\Omega, \qquad R_6 = 8{\cdot}33\ \text{k}\Omega, \qquad E_2 = 4\ \text{V}, \qquad E_3 = -2\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 14(b).

v–i characteristic (v)

Consider the v–i characteristic in Figure 15(a). This is identical to the v–i characteristic (v) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 15(b).

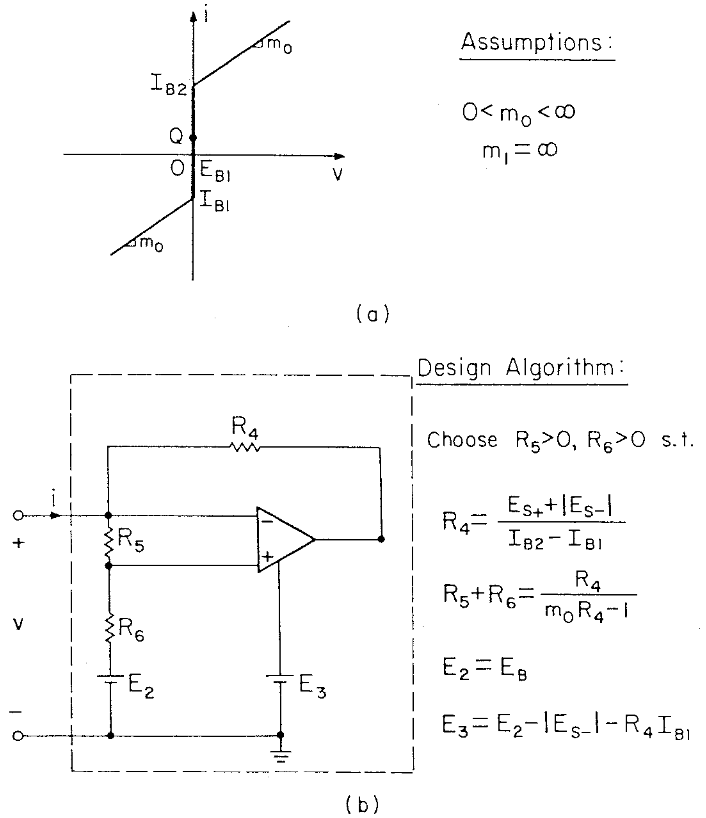


Figure 12. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

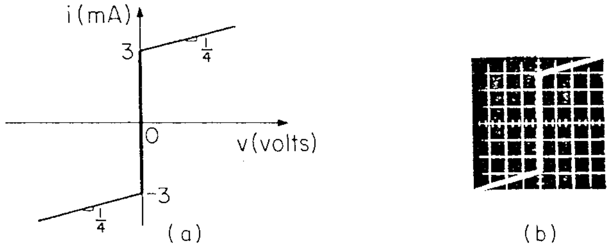


Figure 13. (a) Odd-symmetric characteristic for example 4.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

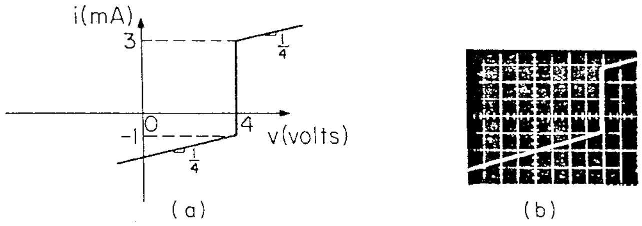


Figure 14. (a) v–i characteristic for example 4.2. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

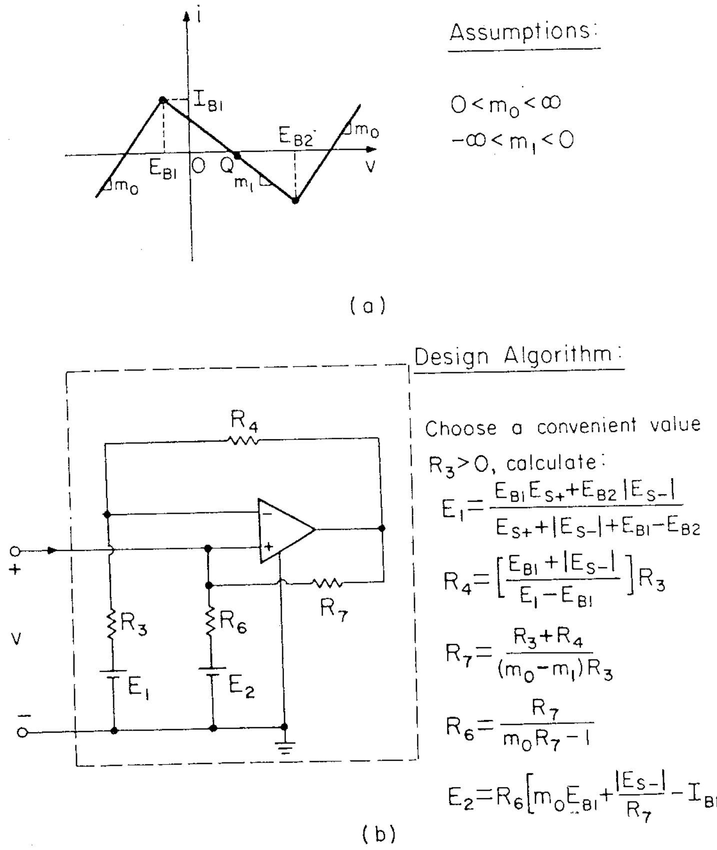


Figure 15. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

Example 5.1 (*odd-symmetric characteristic*). Synthesize the v–i characteristic shown in Figure 16(a) using an op amp with $E_{s+}=15$ V and $E_{s-}=-13$ V. Here $m_0=2$, $m_1=-\frac{1}{2}$, $E_{B1}=-2$ V, $E_{B2}=2$ V and $I_{B1}=1$ mA. Since the slope-breakpoint condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Figure 15(b) are

$$R_3=1\ \text{k}\Omega,\quad R_4=6\ \text{k}\Omega,\quad R_6=608{\cdot}7\ \Omega,\quad R_7=2{\cdot}8\ \text{k}\Omega,\quad E_1=-0{\cdot}167\ \text{V},\quad E_2=-0{\cdot}217\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 16(b).

Example 5.2. Synthesize the v–i characteristic shown in Figure 17(a) using an op amp with $E_{s+}=15$ V and $E_{s-}=-13$ V. Here $m_0=1$, $m_1=-\frac{1}{2}$, $E_{B1}=1$ V, $E_{B2}=2$ V and $I_{B1}=1$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design

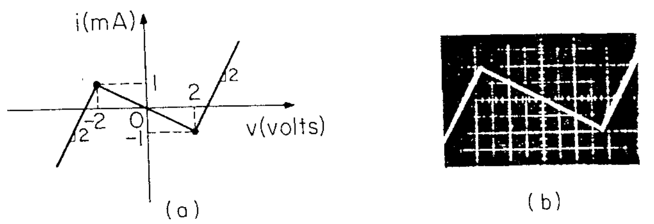


Figure 16. (a) Odd-symmetric characteristic for example 5.1. (b) Measured v–i characteristic. Scale, i: 1 mA/div, v: 1 V/div

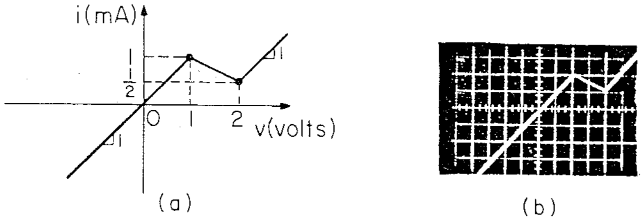


Figure 17. (a) v–i characteristic for example 5.2. (b) Measured v–i characteristic. Scale, i: 1 mA/div, v: 1 V/div

algorithm in Figure 15(b) are

$$R_3 = 1\ \text{k}\Omega, \quad R_4 = 27\ \text{k}\Omega, \quad R_6 = 1{\cdot}06\ \text{k}\Omega, \quad R_7 = 18\ \text{k}\Omega, \quad E_1 = 1{\cdot}52\ \text{V}, \quad E_2 = 0{\cdot}735\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 17(b).

v–i characteristic (vi)

Consider the v–i characteristic in Figure 18(a). This is identical to the v–i characteristic (vi) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 18(b).

Example 6.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 19(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = -2$, $E_{B1} = -3$ V, $E_{B2} = 3$ V and

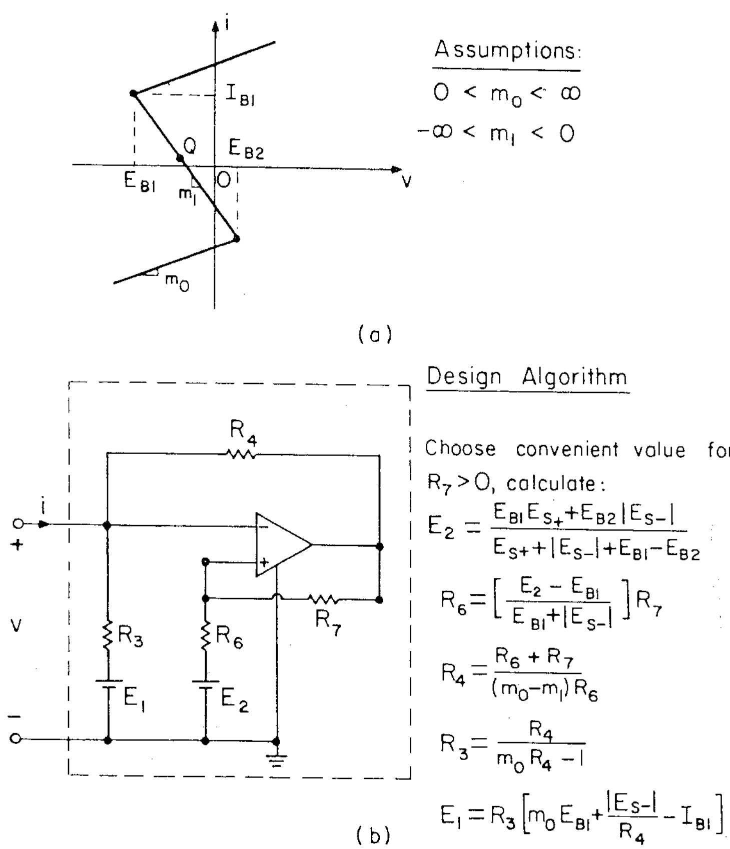


Figure 18. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

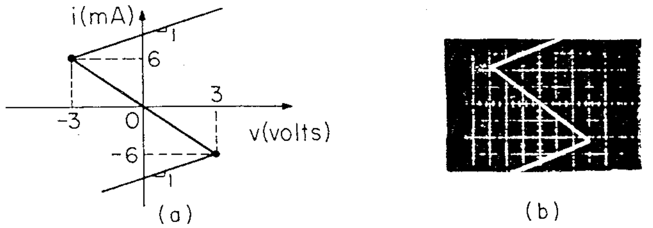


Figure 19. (a) Odd-symmetric characteristic for example 6.1. (b) Measured v–i characteristic. Scale, i: 4 mA/div, v: 2 V/div

$I_{B1} = 6$ mA. Since the slope-breakpoint condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Figure 18(b) are

$$R_3 = 2{\cdot}8\ \text{k}\Omega, \quad R_4 = 1{\cdot}56\ \text{k}\Omega, \quad R_6 = 3\ \text{k}\Omega, \quad R_7 = 11\ \text{k}\Omega, \quad E_1 = -1{\cdot}8\ \text{V}, \quad E_2 = -0{\cdot}273\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 19(b).

Example 6.2. Synthesize the v–i characteristic shown in Figure 20(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = -\frac{1}{2}$, $E_{B1} = 1$ V, $E_{B2} = 3$ V and $I_{B1} = 4$ mA. Condition (1) is satisfied and we know that only positive resistors are needed. The element values calculated from the design algorithm in Figure 18(b) are

$$R_3 = 1{\cdot}12\ \text{k}\Omega, \quad R_4 = 9{\cdot}33\ \text{k}\Omega, \quad R_6 = 1\ \text{k}\Omega, \quad R_7 = 13\ \text{k}\Omega, \quad E_1 = -1{\cdot}8\ \text{V}, \quad E_2 = 2{\cdot}07\ \text{V}$$

The v–i characteristic measurement from the resulting circuit is shown in Figure 20(b).

v–i characteristic (vii)

Consider the v–i characteristic in Figure 21(a). This is identical to the v–i characteristic (vii) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 21(b).

Example 7.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 22(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 2$ V and $I_{B1} = 0$. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 21(b) are

$$R_3 = 1{\cdot}17\ \text{k}\Omega, \quad R_4 = 7\ \text{k}\Omega, \quad R_6 = 1\ \text{k}\Omega, \quad R_7 = 6\ \text{k}\Omega, \quad E_1 = -0{\cdot}17\ \text{V}, \quad E_2 = -0{\cdot}17\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 22(b). Note that since this characteristic is multivalued (i.e. neither voltage-controlled nor current-controlled), we were able to trace only two segments of the v–i characteristic.

Example 7.2. Synthesize the v–i characteristic shown in Figure 23(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 0$, $E_{B1} = -2$ V, $E_{B2} = 4$ V and $I_{B1} = 4$ mA. The slope-breakpoint condition

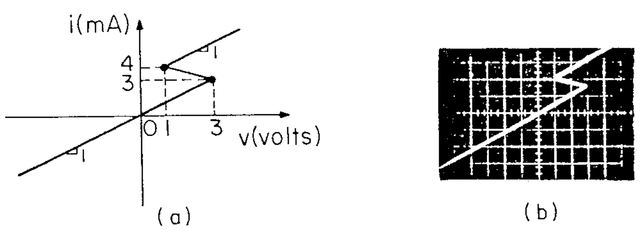
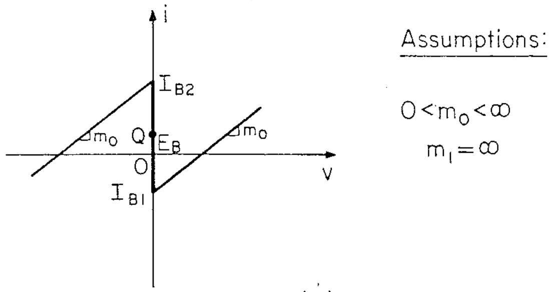


Figure 20. (a) v–i characteristic for example 6.2. (b) Measured v–i characteristic. Scale, i: 4 mA/div, v: 2 V/div



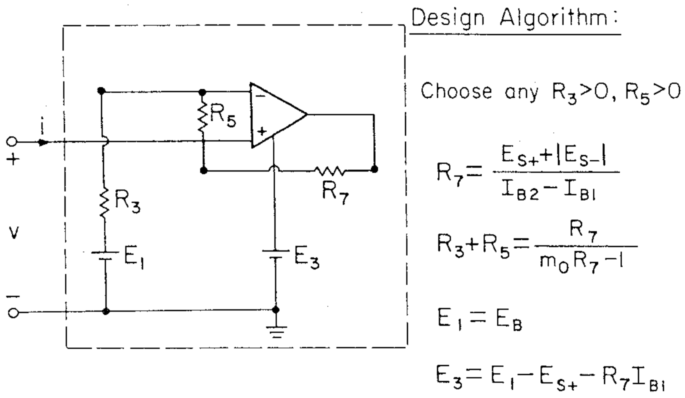


Figure 24. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 21(b) are

$$R_3 = 1{\cdot}27\ \text{k}\Omega,\quad R_4 = 4{\cdot}67\ \text{k}\Omega,\quad R_6 = 3\ \text{k}\Omega,\quad R_7 = 11\ \text{k}\Omega,\quad E_1 = -4{\cdot}09\ \text{V},\quad E_2 = 1\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 23(b). Again only two segments are shown because the characteristic is multivalued.

v–i characteristic (viii)

Consider the v–i characteristic in Figure 24(a). This is identical to the v–i characteristic (viii) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 24(b).

Example 8.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 25(a) using an op amp with $E_{s+} = +15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = \infty$, $I_{B1} = -2$ mA, $I_{B2} = 2$ mA and $E_{B1} = 0$. The slope-breakpoint inequality (2) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 24(b) are

$$R_3 = 167\ \Omega,\quad R_5 = 1\ \text{k}\Omega,\quad R_7 = 7\ \text{k}\Omega,\quad E_2 = 0,\quad E_3 = -1\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 25(b). Note that since this characteristic is multivalued only two segments of the v–i characteristic are shown.

Example 8.2. Synthesize the v–i characteristic shown in Figure 26(a) using an op amp with $E_{s+} = 15$ V, $E_{s-} = -13$ V. Here $m_0 = 1$, $I_{B1} = -1$ mA, $I_{B2} = 3$ mA and $E_{B1} = 6$ V. Since condition (2) is satisfied only

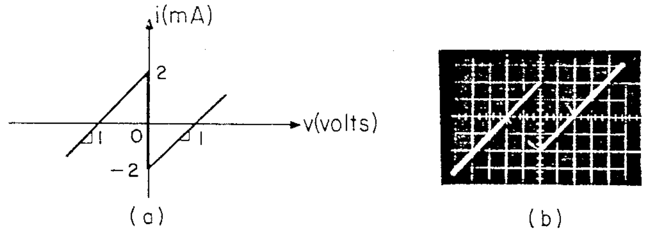


Figure 25. (a) Odd-symmetric characteristic for example 8.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div.

positive resistors are needed. The element values calculated from the design algorithm in Figure 24(b) are

$$R_3 = 167\ \Omega, \quad R_5 = 1\ \text{k}\Omega, \quad R_7 = 7\ \text{k}\Omega, \quad E_2 = 6\ \text{V}, \quad E_3 = -2\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 26(b). Again only two segments are shown because the characteristic is multivalued.

v–i characteristic (ix)

Consider the v–i characteristic in Figure 27(a). This is identical to the v–i characteristic (ix) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 27(b).

Example 9.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 28(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = -3$ V, $E_{B2} = 3$ V and $I_{B1} = -6$ mA. Condition (1) is therefore satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 27(b) are

$$R_2 = 500\ \Omega, \quad R_7 = 2{\cdot}33\ \text{k}\Omega, \quad R_6 = 636{\cdot}4\ \Omega, \quad E_1 = 0\ \text{V}, \quad E_2 = -0{\cdot}273\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 28(b). Note that since this characteristic is multivalued only two segments are shown.

Example 9.2. Synthesize the v–i characteristic shown in Figure 29(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 1$, $m_1 = 2$, $E_{B1} = 2$ V, $E_{B2} = 4$ V and $I_{B1} = -3$ mA. Since condition (1) is satisfied, only positive resistors are needed. The element values calculated from the design algorithm in Figure 27(b) are

$$R_2 = 500\ \Omega, \quad R_7 = 7\ \text{k}\Omega, \quad R_6 = 588{\cdot}5\ \Omega, \quad E_2 = 4{\cdot}23\ \text{V}, \quad E_1 = 3{\cdot}5\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 29(b). Again only two segments are shown because the characteristic is multivalued.

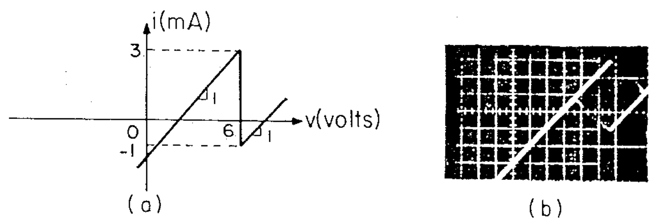


Figure 26. (a) v–i characteristic for example 8.2. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

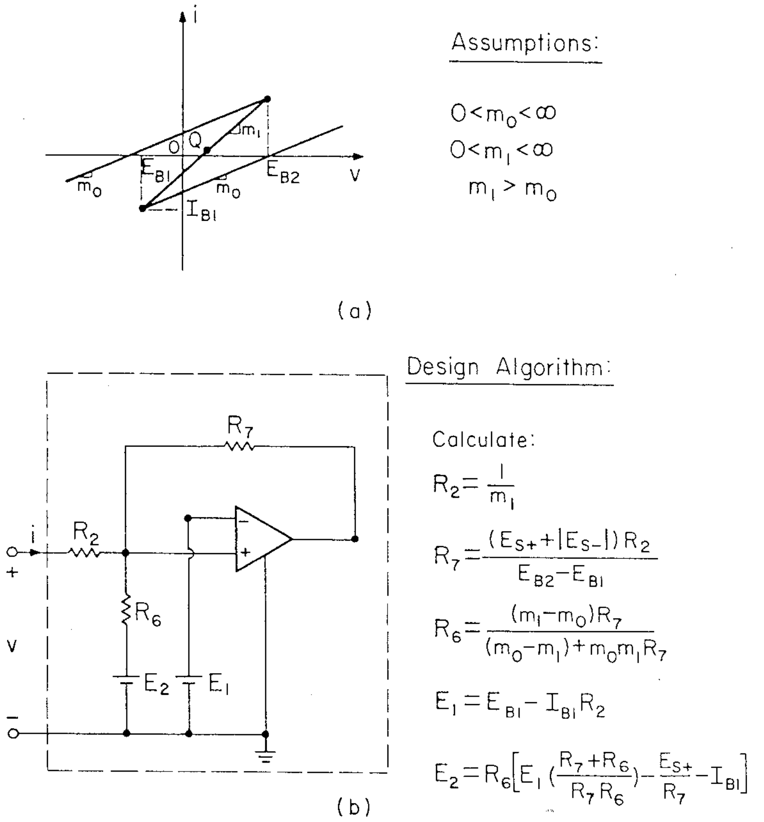


Figure 27. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

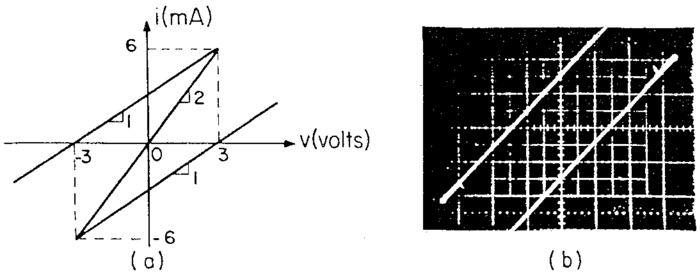


Figure 28. (a) Odd-symmetric characteristic for example 9.1. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

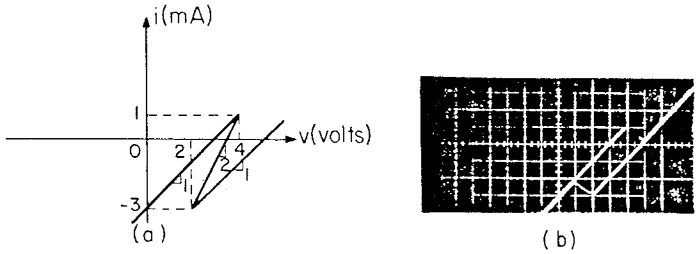


Figure 29. (a) v–i characteristic for example 9.2. (b) Measured v–i characteristic. Scale, i: 2 mA/div, v: 2 V/div

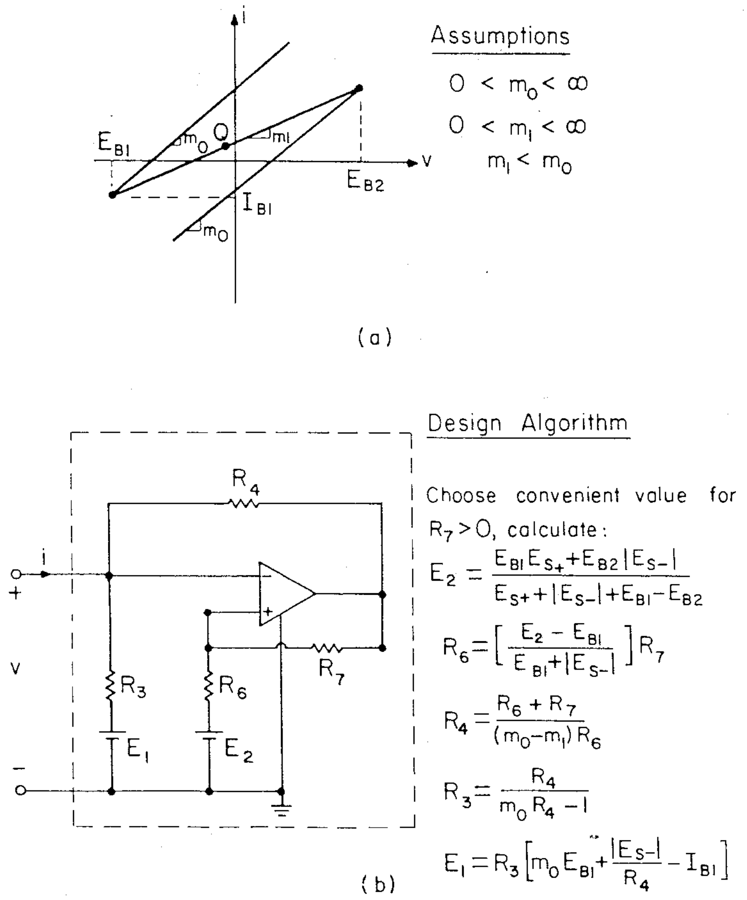


Figure 30. (a) v–i characteristic to be synthesized. (b) Circuit configuration and element values

v–i characteristic (x)

Consider the v–i characteristic in Figure 30(a). This is identical to the v–i characteristic (x) in Figure 1(b) except for a translation of the origin to Q. This characteristic can be synthesized by the circuit in Figure 30(b).

Example 10.1 (odd-symmetric characteristic). Synthesize the v–i characteristic shown in Figure 31(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -4$ V, $E_{B2} = 4$ V and $I_{B1} = -4$ mA. Condition (1) is therefore satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 30(b) are

$$R_3 = 583\ \Omega, \quad R_4 = 3{\cdot}5\ \text{k}\Omega, \quad R_6 = 2\ \text{k}\Omega, \quad R_7 = 5\ \text{k}\Omega, \quad E_1 = -0{\cdot}17\ \text{V}, \quad E_2 = -0{\cdot}4\ \text{V}$$

The v–i characteristic measured from the resulting circuit is shown in Figure 31(b). Since this characteristic is multivalued, only two segments are shown.

Example 10.2. Synthesize the v–i characteristic shown in Figure 32(a) using an op amp with $E_{s+} = 15$ V and $E_{s-} = -13$ V. Here $m_0 = 2$, $m_1 = 1$, $E_{B1} = -4$ V, $E_{B2} = -2$ V and $I_{B1} = -4$ mA. The slope-breakpoint condition (1) is satisfied and only positive resistors are needed. The element values calculated from the design algorithm in Figure 3(b) are

$$R_3 = 518{\cdot}5\ \Omega, \quad R_4 = 14\ \text{k}\Omega, \quad R_6 = 1\ \text{k}\Omega, \quad R_7 = 13\ \text{k}\Omega, \quad E_1 = -1{\cdot}59\ \text{V}, \quad E_2 = -3{\cdot}31\ \text{V}$$

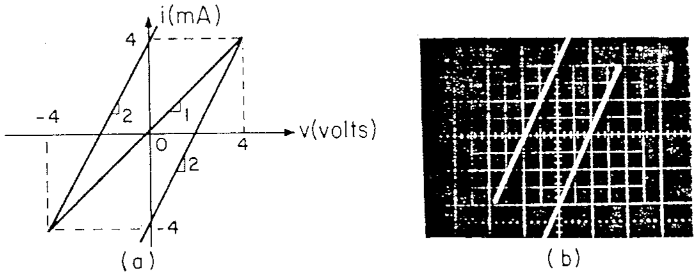


Figure 31. Odd-symmetric characteristic for example 10.1. (b) Measured i–v characteristic. Scale, i: 2 mA/div, v: 2 V/div

The v–i characteristic measured from the resulting circuit is shown in Figure 32(b). Since this characteristic is multivalued, only two segments are shown.

3. PRACTICAL CONSIDERATIONS

In this section we discuss two practical aspects of the circuits presented in Section 2. First, we show that by using an op amp with *identical* saturation voltages no batteries will be needed in realizing any odd-symmetric characteristic in Figure 1(b). Next, we present alternative circuits, for cases where batteries are needed, in which the needed batteries are realized using the power supply voltage.

Realization of odd-symmetric characteristic with circuits containing no batteries

Using an op amp with *identical* saturation voltages, any odd-symmetric characteristic in Figure 1(b) can be realized with circuits containing no batteries. This is easily verified by substituting $E_{s+} = |E_{s-}|$ and $E_{B2} = -E_{B1}$ in the design formulae of Section 2.

In general the saturation voltages of any op amp depend on the power supply voltages v_{cc+} and v_{cc-} required for the op amp operation. In the case of the 741 op amp the positive saturation voltage $E_{s+} = v_{cc+}$ but the negative saturation voltage is considerably lower (up to 2 V) than v_{cc-}.[10] However, by adjusting v_{cc+} the two saturation voltages can be made identical. Recall that all the examples in Section 2 were obtained by using $v_{cc+} = 15$ V, $v_{cc-} = -15$ V, which correspond to $E_{s+} = 15$ V and $E_{s-} = -13$ V. However, using $v_{cc+} = 13$ V and $v_{cc-} = -15$ V we were able to obtain $E_{s+} = |E_{s-}| = 13$ V. This op amp was then used to realize the same odd-symmetric characteristics presented as examples in Section 2. These measured characteristics along with the resistor values are exhibited in Figures 33–42.

Alternative circuits

In order to produce the v–i characteristic of any circuit shown in Section 2, four power supplies are needed: two power supplies v_{cc+}, v_{cc-} for op amp operation and the other two as batteries. From a practical point of view this is sometimes undesirable. Hence, in what follows alternative circuits are presented in

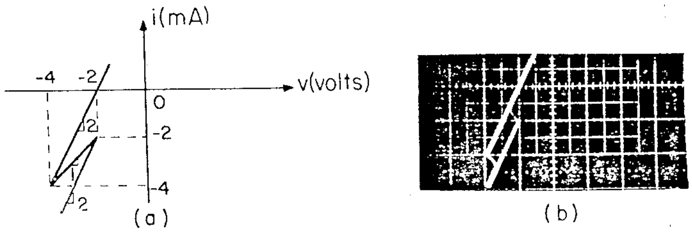


Figure 32. (a) v–i characteristic for example 10.2. (b) Measured i–v characteristic. Scale, i: 2 mA/div, v: 2 V/div

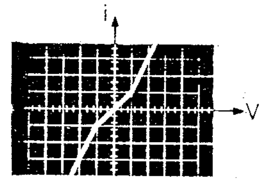


Figure 33. Odd-symmetric characteristic from Example 1.1 realized using an op amp with identical saturation voltages in Figure 3(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 12\ \text{k}\Omega$, $R_6 = 520\ \Omega$ and $R_7 = 13\ \text{k}\Omega$. Scale, i: 2 mA/div, v: 2 V/div

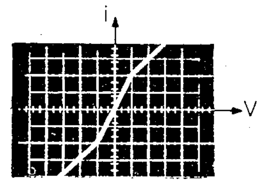


Figure 34. Odd-symmetric characteristic from example 2.1 realized using an op amp with identical saturation voltages in Figure 6(b) with $R_1 = 500\ \Omega$, $R_3 = 590{\cdot}9\ \Omega$, $R_4 = 3{\cdot}25\ \text{k}\Omega$. Scale, i: 4 mA/div, v: 4 V/div

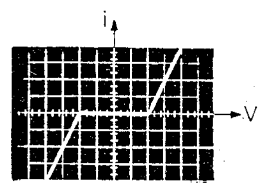


Figure 35. Odd-symmetric characteristic from example 3.1 realized using an op amp with identical saturation voltages in Figure 9(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 2{\cdot}5\ \text{k}\Omega$, $R_6 = 590{\cdot}9\ \Omega$, and $R_7 = 3{\cdot}25\ \text{k}\Omega$. Scale, i: 2 mA/div, v: 2 V/div

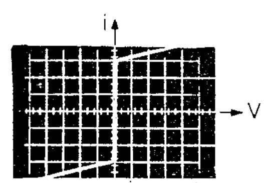


Figure 36. Odd-symmetric characteristic from example 4.1 realized using an op amp with identical saturation voltages in Figure 12(b) with $R_4 = 4{\cdot}33\ \text{k}\Omega$, $R_5 = 26\ \text{k}\Omega$ and $R_6 = 26\ \text{k}\Omega$. Scale, i: 2 mA/div, v: 2 V/div

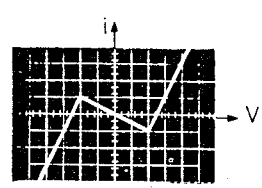


Figure 37. Odd-symmetric characteristic from example 5.1 realized using an op amp with identical saturation voltages in Figure 15(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 5{\cdot}5\ \text{k}\Omega$, $R_6 = 619\ \Omega$ and $R_7 = 2{\cdot}6\ \text{k}\Omega$. Scale, i: 2 mA/div, v: 2 V/div

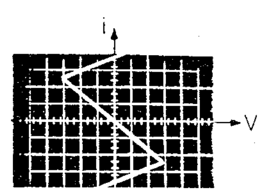


Figure 38. Odd-symmetric characteristic from example 6.1 realized using an op amp with identical saturation voltages in Figure 18(b) with $R_3 = 3{\cdot}25\ \text{k}\Omega$, $R_4 = 1{\cdot}44\ \text{k}\Omega$, $R_6 = 1\ \text{k}\Omega$ and $R_7 = 3{\cdot}33\ \text{k}\Omega$. Scale, i: 5 mA/div, v: 2 V/div

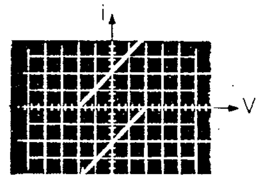


Figure 39. Odd-symmetric characteristic from example 7.1 realized using an op amp with identical saturation voltages in Figure 21(b) with $R_3 = 1{\cdot}18\,\mathrm{k\Omega}$, $R_4 = 6{\cdot}5\,\mathrm{k\Omega}$, $R_6 = 1\,\mathrm{k\Omega}$ and $R_7 = 5{\cdot}5\,\mathrm{k\Omega}$. Scale, i: 2 mA/div, v: 2 V/div

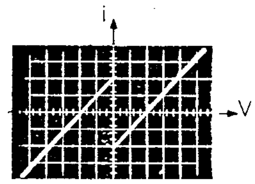


Figure 40. Odd-symmetric characteristic from example 8.1 realized using an op amp with identical saturation voltages in Figure 24(b) with $R_3 = 1\,\mathrm{k\Omega}$, $R_5 = 154\,\Omega$ and $R_7 = 6{\cdot}5\,\mathrm{k\Omega}$. Scale, i: 2 mA/div, v: 2 V/div

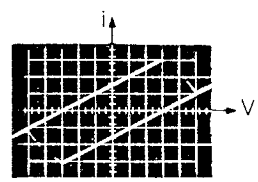


Figure 41. Odd-symmetric characteristic from example 9.1 realized using an op amp with identical saturation voltages in Figure 27(b) with $R_1 = 500\,\Omega$, $R_3 = 650\,\Omega$ and $R_4 = 2{\cdot}167\,\mathrm{k\Omega}$. Scale, i: 4 mA/div, v: 2 V/div

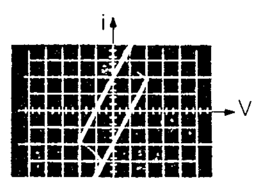


Figure 42. Odd-symmetric characteristic from example 10.1 realized using an op amp with identical saturation voltages in Figure 30(b) with $R_3 = 590{\cdot}9\,\Omega$, $R_4 = 3{\cdot}25\,\mathrm{k\Omega}$, $R_6 = 1\,\mathrm{k\Omega}$ and $R_7 = 2{\cdot}25\,\mathrm{k\Omega}$. Scale, i: 4 mA/div, v: 4 V/div

which the two batteries are realized by direct use of the op amp power supplies. The only restriction is that the battery voltages $|E_1|$ and $|E_2|$ must be less than the power supply voltages.

First, consider the circuit in Figure 43. This circuit can be used to realize any battery E_1 less than the supply voltage E_s by choosing appropriate values for R_A and R_B.

Figure 44 shows the circuit modification needed to realize a series combination of a resistor and a battery, as in the circuits from Section 2, using the power supply.

The circuit modification needed to realize a battery which is directly connected to input terminals of an op amp using the power supply is shown in Figure 45.

4. APPLICATIONS

This section is devoted to the design of several practical circuits using the simplified canonical circuits from Section 2 as building blocks.

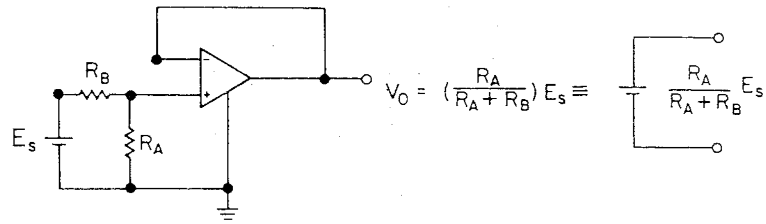


Figure 43. Circuit for realizing a battery using the power supply voltages

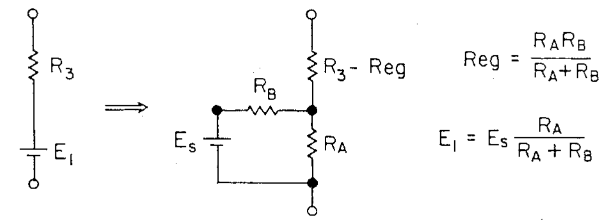


Figure 44. Circuit transformation to realize a series combination of a resistor and a battery using the power supply voltage

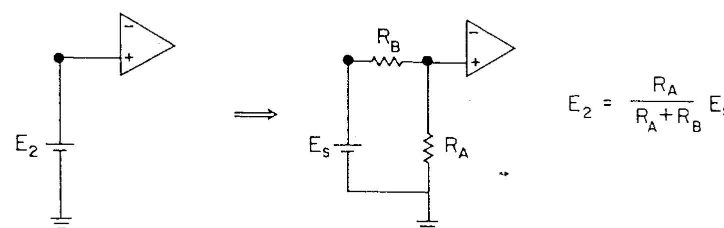


Figure 45. Circuit transformation to realize a battery directly connected to the op amp input terminal using the power supply voltage

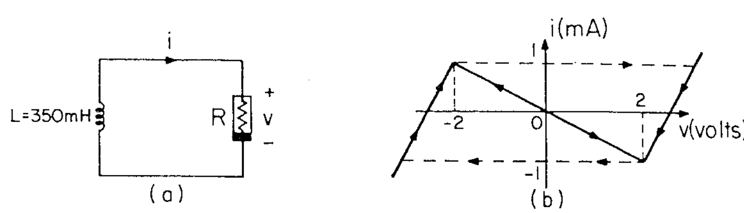


Figure 46. (a) The circuit for a soft oscillator. (b) v–i characteristic for R

A soft oscillator

Consider the circuit in Figure 46(a) where the non-linear resistor has a voltage controlled v–i characteristic as in Figure 46(b). The dynamic route in Figure 46(b) shows that regardless of the initial flux on the inductor the circuit exhibits oscillations. The measured v–i characteristic and the measured oscillations are shown in Figure 47.

A hard oscillator

Consider the circuit in Figure 48(a) where the parallel combination of R_1 and R_2 has a v–i characteristic as shown in Figure 48(b). The dynamic route in Figure 48(b) reveals that the origin is a stable equilibrium

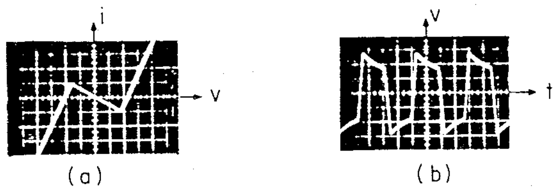


Figure 47. (a) Measured v–i characteristic for R realized using Figure 15(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 5{\cdot}5\ \text{k}\Omega$, $R_6 = 619\ \Omega$ and $R_7 = 2{\cdot}6\ \text{k}\Omega$. Scale, i: 2 mA/div, v: 2 V/div. (b) Measured voltage oscillations. Scale, v: 2 V/div, t: 200 μs/div

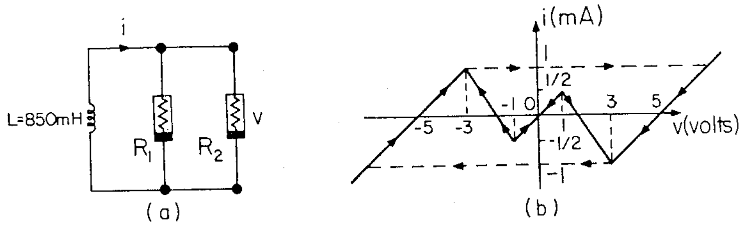


Figure 48. (a) Circuit for a hard oscillator. (b) v–i characteristic for the parallel combination of R_1 and R_2

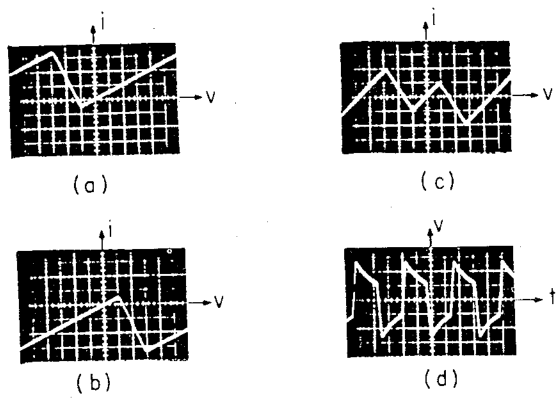


Figure 49. (a) Measured v–i characteristic for R_1 using Figure 15(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 13\ \text{k}\Omega$, $R_6 = 6{\cdot}22\ \text{k}\Omega$, $R_7 = 11{\cdot}2\ \text{k}\Omega$, $E_1 = -2{\cdot}23$ V and $E_2 = 8{\cdot}33$ V. Scale, i: 1 mA/div, v: 2 V/div. (b) Measured v–i characteristic for R_2 using Figure 15(b) with $R_3 = 1\ \text{k}\Omega$, $R_4 = 13\ \text{k}\Omega$, $R_6 = 6{\cdot}22\ \text{k}\Omega$, $R_7 = 11{\cdot}2\ \text{k}\Omega$, $E_1 = 2{\cdot}07$ V and $E_2 = 7{\cdot}22$ V. Scale, i: 1 mA/div, v: 2 V/div. (c) Measured v–i characteristic for the parallel combination of R_1 and R_2. Scale, i: 1 mA/div, v: 2 V/div. (d) Measured oscillations. Scale, v: 5 V/div, t: 500 μs/div

point. Therefore, in order to obtain oscillations an initial current of $i_L(0) > \frac{1}{2}$ mA must be imposed on the inductor. The measured characteristics for R_1 and R_2 are shown in Figures 49(a) and (b), the parallel combination of these two is shown in Figure 49(c) and the measured oscillation is exhibited in Figure 49(d).

A 3-state circuit

Consider the circuit in Figure 50(a) where the parallel combination of the two non-linear resistors results in a v–i characteristic as shown in Figure 50(b). From the associated dynamic route we see that Q_1, Q_2 and Q_3 are all stable equilibrium points. Therefore, depending on the initial charge on the capacitor one of three states will be reached. The measured v–i characteristic along with the circuit used in the realization is shown in Figure 51.

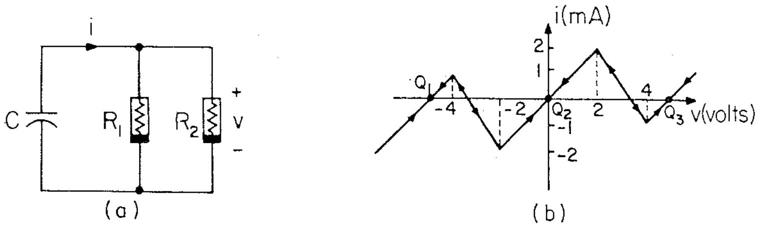


Figure 50. (a) A three-state circuit. (b) v–i characteristic for the parallel combination of R_1 and R_2

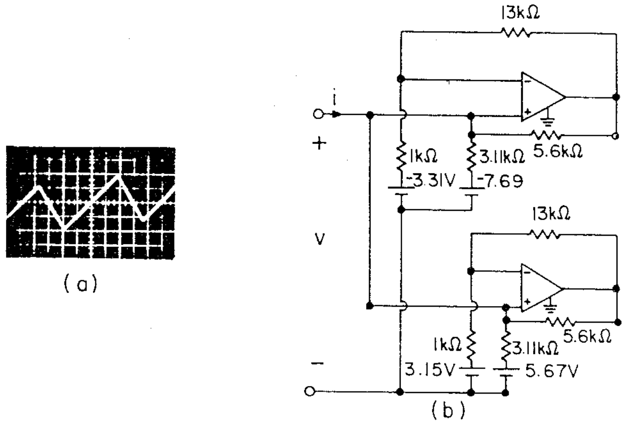


Figure 51. (a) Measured v–i characteristic for the parallel combination of R_1 and R_2. (b) Circuit used to measure v–i characteristic in (a)

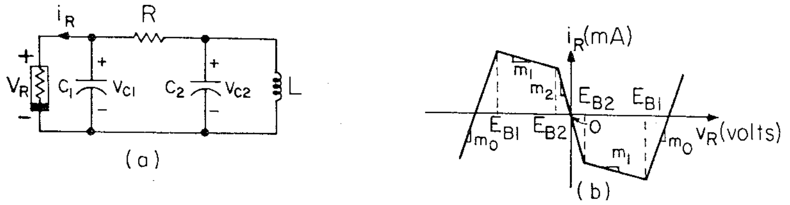


Figure 52. (a) A chaotic circuit. (b) v–i characteristic for R

A chaotic circuit

Roughly speaking, a circuit is *chaotic* iff its solution is neither a periodic (possibly constant) nor an almost periodic function. It is now widely believed that a large class of practical non-linear circuits can become chaotic if the circuit parameters are appropriately chosen.

The circuit in Figure 52(a) has recently been shown to exhibit chaotic behaviour.[11] The non-linear resistor in this circuit must have a v–i characteristic as in Figure 52(b). In the following we present the design procedure for obtaining such a characteristic. A parallel combination of two odd-symmetric voltage-controlled characteristics is needed in the synthesis. Consider the characteristics in Figure 53; in order for the parallel combination of these two characteristics to result in a characteristic as in Figure 52(b) we need

$$m_{01}+m_{02}=m_0 \tag{3}$$

$$m_{02}+m_{11}=m_1 \tag{4}$$

$$m_{11}+m_{12}=m_2 \tag{5}$$

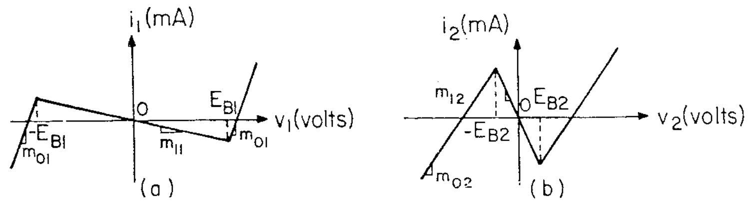


Figure 53. Two v–i characteristics needed to realize R in Figure 52

To solve these equations choose $|m_{12}|>|m_{11}|$ so that (5) is satisfied. Then

$$m_{02}=m_1-m_{11}$$

$$m_{01}=m_0-m_1+m_{11}$$

Hence, to realize the characteristic in Figure 52(b) we have to realize R_1 with parameters (m_{01}, m_{11}, E_{B1}) and R_2 with parameters (m_{02}, m_{12}, E_{B2}) using the design algorithms from Section 2.

Remark

We choose $|m_{12}|>|m_{11}|$ in order to satisfy condition (1) of Section 2. This is due to the fact that E_{B1} is quite large and we need a small m_{11} in order to satisfy the slope-breakpoint inequality.

Example

Realize the characteristic shown in Figure 52(b) with $m_0=5$, $m_1=-0{\cdot}1$, $m_2=-4$, $E_{B1}=11$ and $E_{B2}=+1$. Substituting these parameters into equations (3)–(5) we get

$$m_{01}+m_{02}=5$$

$$m_{02}+m_{11}=-0{\cdot}1$$

$$m_{11}+m_{12}=-4$$

Choose $m_{11}=-0{\cdot}5$, $m_{12}=-3{\cdot}5$. Then,

$$m_{01}=4{\cdot}6,\ m_{02}=0{\cdot}4$$

Therefore, we have to realize R_1 with $(m_{01}=4{\cdot}6, m_{11}=-0{\cdot}5, E_{B1}=11)$ and R_2 with $(m_{02}=0{\cdot}4, m_{11}=-3{\cdot}5, E_{B2}=1)$. This was done using op amps with identical saturation voltages $E_{s+}=|E_{s-}|=13$. The measured characteristic for R_1 and R_2 is shown in Figures 54(a) and (b). The measured characteristic resulting from the parallel combination of these two is shown in Figure 54(c). Figure 54(d) is the circuit used in these realizations.

Connecting the one-port in Figure 54(d) in place of the non-linear resistor in Figure 52(a), and using appropriate values of R, L, C_1 and C_2, an interesting chaotic attractor is observed and has been reported in References 12 and 13. This is one example where a prescribed piecewise-linear negative differential resistance characteristic must be precisely synthesized.

5. THEORY

In this section we present the circuit-theoretic approach from which the canonical circuit in Figure 2 is derived. First, the problem of synthesizing op amp circuits is reduced to that of synthesizing a 3×3 conductance matrix. Next, the concept of a *paramount* matrix is introduced. Finally, the fact that a 3×3 conductance matrix is realizable using linear positive resistors iff it is paramount, is used to derive the canonical circuit.

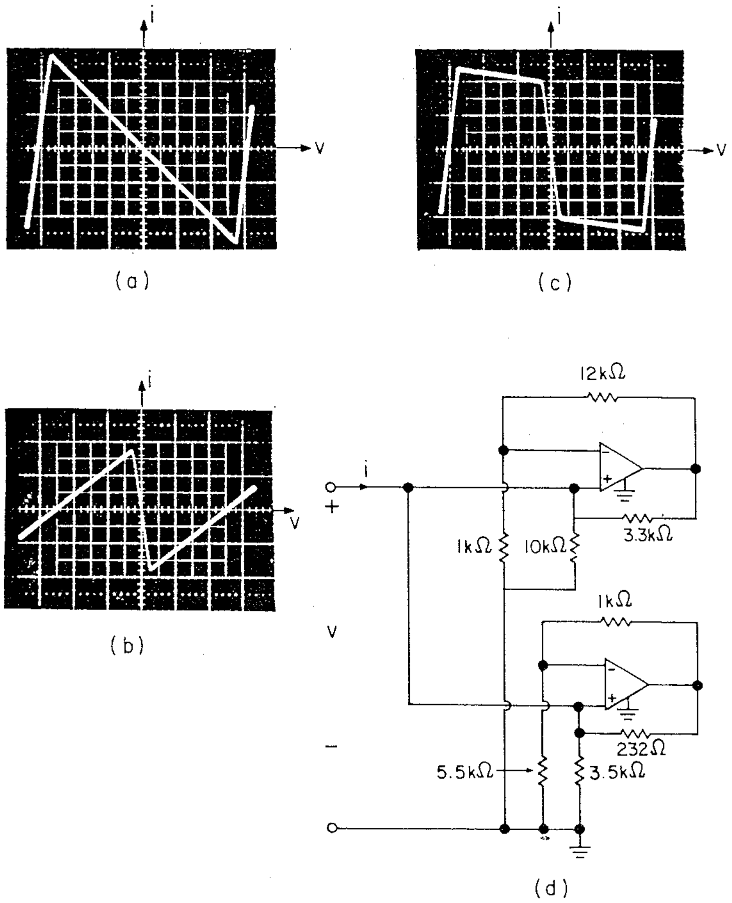


Figure 54. (a), (b) Measured v–i characteristics for R_1 and R_2 in the chaotic circuit example. Scale, i: 2 mA/div, v: 4 V/div. (c) Measured v–i characteristic for parallel combination of (a) and (b) representing R in the chaotic circuit. (d) Circuit used in these measurements

5.1. *Circuit formulation*

Consider a general circuit containing one op amp, linear positive resistors and independent voltage sources as shown in Figure 55. Next, replace the op amp by its piecewise-linear model as in Figure 56(a), where the 2-terminal non-linear resistor is characterized by Figure 56(b). The resulting circuit is shown in Figure 57. Note that for simplicity we use an op-amp model with saturation voltages E_{s+} and E_{s-} of equal magnitude. The following results apply equally well, *mutatis mutandis*, when $E_{s+} \neq |E_{s-}|$. Since the 3-port N in Figure 57 contains only 2-terminal resistors and independent sources, it is *reciprocal.* Let N

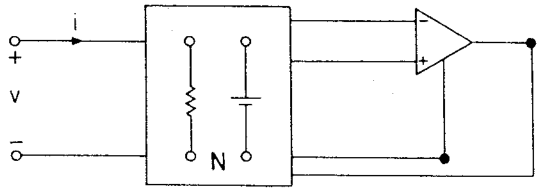
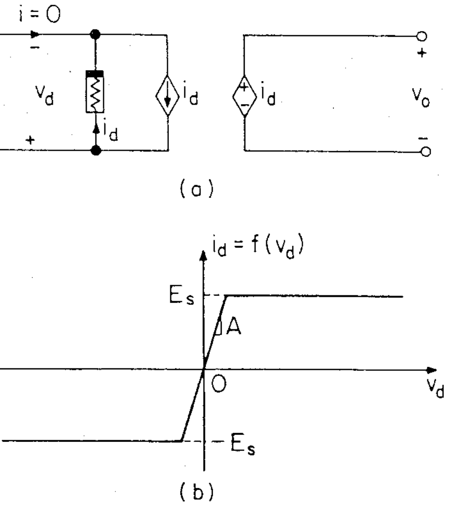
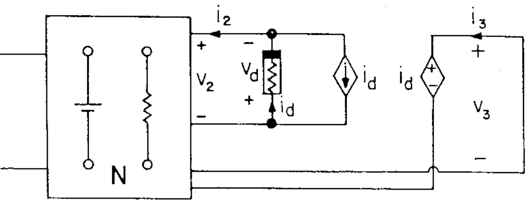


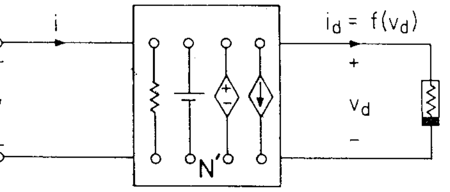
Figure 55. General circuit containing one op amp resistors and batteries



re 56. Piecewise-linear circuit model for an op amp



ned by replacing the op amp in Figure 55 with the model in Figure 56



btained by pulling out the only non-linear element in Figure 57.

tage-controlled representation:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{12} & g_{22} & g_{23} \\ g_{13} & g_{23} & g_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \tag{6}$$

rocal. Next, consider the circuit in Figure 58, which is obtained from non-linear element. Comparing the circuits in Figures 57 and 58 and g transmission (chain) representation for the 2-port N' (assuming that

$$\left.\begin{aligned} &-\frac{g_{11}g_{23}}{g_{12}}\Big) i_d + \left(\frac{g_{11}g_{22}}{g_{12}} - g_{12}\right) v_d + \left(I_1 - \frac{g_{11}}{g_{12}} I_2\right) \\ &i_d + \frac{g_{22}}{g_{12}} v_d - \frac{1}{g_{12}} I_2 \end{aligned}\right\} \tag{7}$$

We are now ready to present explicit equations describing the driving point characteristic of any circuit containing one op amp, linear positive resistors and independent voltage sources.

Theorem 1

Hypotheses

(1) $A \to \infty$ in Figure 56(b), i.e. assume an ideal op-amp model.
(2) The 3-port N in Figure 55 has a short-circuit conductance matrix $\mathbf{G}$.

Conclusion. The *driving-point characteristic* of the one op-amp circuit in Figure 55 consists of 3 connected *piecewise-linear* segments. If we label these segments consecutively by 1, 2 and 3, then segments 1 and 3 are *parallel* to each other. Each segment is described by the following linear equation and interval of validity:

Segment 1

$$i=\left(\frac{g_{11}g_{22}-g_{12}^2}{g_{22}}\right)v+E_s\left(\frac{g_{12}g_{23}-g_{13}g_{22}}{g_{22}}\right)+I_1-\frac{g_{12}}{g_{22}}I_2 \tag{8a}$$

where

$$\left.\begin{array}{ll} -\infty < i \leq E_s\left(\dfrac{g_{11}g_{23}-g_{12}g_{13}}{g_{12}}\right), & \text{if } \dfrac{g_{11}g_{22}-g_{12}^2}{g_{12}}>0 \\ E_s\left(\dfrac{g_{11}g_{23}-g_{12}g_{13}}{g_{12}}\right)\leqslant i<\infty, & \text{if } \dfrac{g_{11}g_{22}-g_{12}^2}{g_{12}}<0 \\ -\infty<v\leq E_s\dfrac{g_{23}}{g_{12}}, & \text{if } g_{12}>0 \\ E_s\dfrac{g_{23}}{g_{12}}\leq v<\infty, & \text{if } g_{12}<0 \end{array}\right\} \tag{8b}$$

Segment 2

$$i=\left(\frac{g_{11}g_{23}-g_{12}g_{13}}{g_{23}}\right)v+I_1-\frac{g_{13}}{g_{23}}I_2 \tag{9a}$$

where

$$\left.\begin{array}{ll} -E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right)\leqslant i\leqslant E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right), & \text{if } \dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}>0 \\ E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right)\leqslant i\leqslant -E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right), & \text{if } \dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}<0 \\ -E_s\dfrac{g_{23}}{g_{12}}\leqslant v\leqslant E_s\dfrac{g_{23}}{g_{12}}, & \text{if } \dfrac{g_{23}}{g_{12}}>0 \\ E_s\dfrac{g_{23}}{g_{12}}\leqslant v\leqslant -E_s\dfrac{g_{23}}{g_{12}}, & \text{if } \dfrac{g_{23}}{g_{12}}<0 \end{array}\right\} \tag{9b}$$

Segment 3

$$i=\left(\frac{g_{11}g_{22}-g_{12}^2}{g_{22}}\right)v-E_s\left(\frac{g_{12}g_{23}-g_{13}g_{22}}{g_{22}}\right)+I_1-\frac{g_{12}}{g_{22}}I_2 \tag{10a}$$

where

$$\left.\begin{array}{ll} E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right)\leq i<\infty, & \text{if } \dfrac{g_{11}g_{22}-g_{12}^2}{g_{12}}>0 \\ -\infty<i\leq E_s\left(\dfrac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}\right), & \text{if } \dfrac{g_{11}g_{22}-g_{12}}{g_{12}}<0 \\ -E_s\dfrac{g_{23}}{g_{12}}\leq v<\infty, & \text{if } g_{12}>0 \\ -\infty<v\leq -E_s\dfrac{g_{23}}{g_{12}}, & \text{if } g_{12}<0 \end{array}\right\} \tag{10b}$$

Proof. For $-\infty<v_d\leq -(E_s/A)$ we have $i_d=-E_s$. Substituting for i_d in (7) and solving for v_d we get

$$\left.\begin{array}{l} v_d=\dfrac{i-I+E_s k_{11}}{k_{12}}, \\ v_d=\dfrac{v-V+E_s k_{21}}{k_{22}}, \end{array} \quad -\infty<v_d\leq -\dfrac{E_s}{A}\right\} \tag{11}$$

where

$$k_{11}=\frac{g_{12}g_{13}-g_{11}g_{23}}{g_{12}}, \qquad k_{12}=\frac{g_{11}g_{22}-g_{12}^2}{g_{12}}, \qquad I=I_1-\frac{g_{11}}{g_{12}}I_2$$

$$k_{21}=-\frac{g_{23}}{g_{12}}, \qquad k_{22}=\frac{g_{22}}{g_{12}}, \qquad V=\frac{-1}{g_{12}}I_2$$

Solving for i in terms of v in (11) and letting $A\to\infty$ we obtain equations (8). A similar procedure yields equations (9) and (10).

Our next result characterizes the properties of the driving-point characteristics of the piecewise-linear resistive one port shown in Figure 59. First, we state the general case. The special case for op amp circuits will follow as a Corollary.

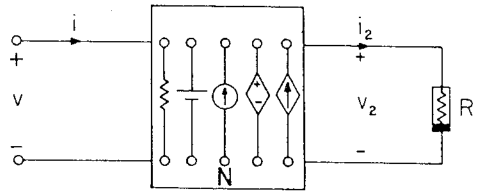


Figure 59. Circuit for Theorem 2

Theorem 2

Consider the non-linear resistor terminated one-port shown in Figure 59. Let R be an n-segment piecewise-linear voltage-controlled resistor described by the canonical equation[4]

$$i_2=a_0+a_1v_2+c_1|v_2-b_1|+\ldots+c_n|v_2-b_n| \tag{12}$$

Let N be the two-port containing linear resistors, independent sources and linear controlled sources. Let N be described by the following transmission representation:

$$i=k_{11}i_2+k_{12}v_2+I$$

$$v=k_{21}i_2+k_{22}v_2+V$$

Then, the v–i driving-point characteristic is

(a) *Strictly monotone-increasing* if and only if

$$k_{12}+k_{11}\left(a_1+\sum_{l=1}^{k} c_l-\sum_{l=k+1}^{n} c_l\right)>0 \text{ (or all } <0)$$

and

$$k_{22}+k_{21}\left(a_1+\sum_{l=1}^{k} c_l-\sum_{l=k+1} c_l\right)>0 \text{ (or all } <0) \tag{13}$$

for all $k=0, 1, 2, \ldots, n$.

(b) *Current-controlled* if and only if

$$k_{12}+k_{11}\left(a_1+\sum_{l=1}^{k} c_l-\sum_{l=k+1}^{n} c_l\right)>0 \text{ (or all } <0) \quad \text{for all } k=0, 1, 2, \ldots, n \tag{14}$$

(c) *Voltage-controlled* if and only if

$$k_{22}+k_{21}\left(a_1+\sum_{l=1}^{k} c_l-\sum_{l=k+1}^{n} c_l\right)>0 \text{ (or all } <0) \text{ for all } k=0, 1, 2, \ldots, n \tag{15}$$

Furthermore, the driving-point characteristic is multivalued (i.e. neither voltage-controlled nor current-controlled) if neither one of (13), (14) nor (15) is satisfied.

Proof. An outline of the proof is as follows. First, using a similar procedure as in the proof of Theorem 1 we derive the driving-point characteristic which consists of n different segments. Then, using the fact that for a characteristic to be, for example, current-controlled, the range of the current for each segment should not overlap, we obtain conditions (13)–(15).

Corollary

The driving-point characteristic of a single op-amp circuit (i.e. (8)–(10)) is

(a) *Strictly monotone-increasing* if and only if

$$\left.\begin{array}{r} g_{23}<0 \\ g_{11}g_{23}-g_{12}g_{13}<0 \end{array}\right\} \tag{16}$$

(b) *Solely current-controlled* if and only if

$$\left.\begin{array}{r} g_{23}>0 \\ g_{11}g_{23}-g_{12}g_{13}<0 \end{array}\right\} \tag{17}$$

(c) *Solely voltage-controlled* if and only if

$$\left.\begin{array}{r} g_{23}<0 \\ g_{11}g_{23}-g_{12}g_{13}>0 \end{array}\right\} \tag{18}$$

(d) *Multivalued* if and only if

$$\left.\begin{array}{r} g_{23}>0 \\ g_{11}g_{23}-g_{12}g_{13}>0 \end{array}\right\} \tag{19}$$

Proof. The proof is a special case of the proof of Theorem 2.

5.2. Paramountcy

An $n \times n$ symmetric matrix **G** is said to be *paramount* iff each principal minor of order m is *not* less than the absolute value of any mth order minor built from the same rows (or columns), where $m=$

$1, 2, \ldots, n-1$.[8] In particular for a 3×3 matrix we have the following conditions:

$$\mathbf{G} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{12} & g_{22} & g_{23} \\ g_{13} & g_{23} & g_{33} \end{bmatrix}$$

$$\text{conditions involving first-order minors} \begin{cases} g_{11} \geqslant |g_{12}|, \; g_{11} \geqslant |g_{13}| \\ g_{22} \geqslant |g_{12}|, \; g_{22} \geqslant |g_{23}| \\ g_{33} \geqslant |g_{13}|, \; g_{33} \geqslant |g_{23}| \end{cases}$$

$$\text{conditions involving second-order minors} \begin{cases} \Delta_{11} \geqslant |\Delta_{13}|, \; \Delta_{11} \geqslant |\Delta_{12}| \\ \Delta_{22} \geqslant |\Delta_{21}|, \; \Delta_{22} \geqslant |\Delta_{23}| \\ \Delta_{33} \geqslant |\Delta_{31}|, \; \Delta_{33} \geqslant |\Delta_{32}| \end{cases}$$

where

Δ_{ij} = determinant of the submatrix obtained by deleting row i and column j.

An example of a paramount matrix is shown below.

$$\mathbf{G} = \begin{bmatrix} 3 & 2 & -2 \\ 2 & 2 & -1 \\ -2 & -1 & 2 \end{bmatrix} \quad \begin{matrix} \Delta_{11} = 3, & |\Delta_{12}| = |\Delta_{21}| = 2 \\ \Delta_{22} = 2, & |\Delta_{13}| = |\Delta_{31}| = 2 \\ \Delta_{33} = 2, & |\Delta_{23}| = |\Delta_{32}| = 1 \end{matrix}$$

The inverse of a non-singular paramount matrix is also paramount. Paramountcy is a weaker condition than diagonal dominancy but a stronger condition than positive definiteness.

5.3. *Canonical circuit*

It has been shown[8] that a necessary and sufficient condition for a 3×3 matrix to be realizable as a short-circuit admittance of a 3-port resistive network made of positive linear resistances is that it be a paramount matrix. In this subsection we use this fact to systematically derive the canonical circuit in Figure 2.

Consider any of the odd-symmetric driving-point characteristics in Figure 1(b). Comparing equations (8)–(10) with any of these characteristics we obtain the following equations. (Note that we are assuming no batteries, i.e. $I_1 = I_2 = 0$ in (8)–(10).)

$$m_0 = m_2 = \frac{g_{11}g_{22} - g_{12}^2}{g_{22}} \tag{20}$$

$$m_1 = \frac{g_{11}g_{23} - g_{12}g_{13}}{g_{23}} \tag{21}$$

$$E_B = E_s\left(\frac{g_{23}}{g_{12}}\right) \tag{22}$$

We are now ready to present the algorithm for synthesizing any of the characteristics in Figure 1(b).

Step 1. Using (20)–(22) find a paramount **G** matrix. Two parameters can be chosen arbitrarily. However, the above Corollary must also be taken into account, i.e. **G** must satisfy the appropriate inequalities (16), (17), (18) or (19).

Step 2. Realize the **G** matrix from Step 1. An algorithm for accomplishing this task is given in Reference 8. We need at most six positive linear resistors. The 3-port shown in Figure 60 can be used to realize any 3×3 paramount conductance matrix.

Step 3. Connect the 3-port obtained in Step 2 to an op amp and complete the synthesis procedure.

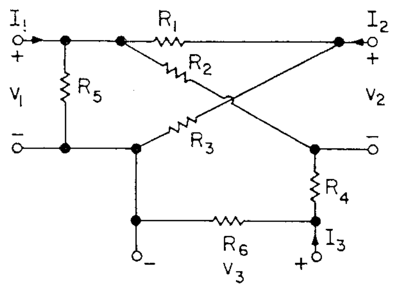


Figure 60. This 3-port can be used to realize any 3×3 paramount conductance matrix with positive resistors

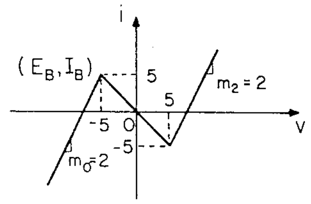


Figure 61. v–i characteristic to be realized using the algorithm in Section 5

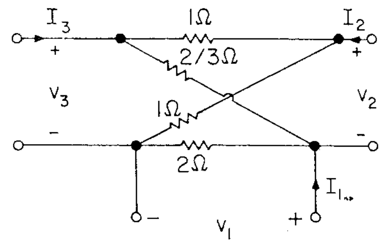


Figure 62. A realization of the **G** matrix in the above example

Example

For the characteristic shown in Figure 61 we have

$$m_0 = 2, \qquad m_1 = -1, \qquad E_B = -5$$

Assume $E_s = 10$ V.

Step 1. Choose $g_{22} = g_{12} = 2$, then (20)–(22) yield

$$g_{23} = -1, \qquad g_{11} = 4, \qquad g_{13} = -\tfrac{5}{2}$$

Hence

$$\mathbf{G} = \begin{bmatrix} 4 & 2 & -5/2 \\ 2 & 2 & -1 \\ -5/2 & -1 & 5/2 \end{bmatrix}$$

which is paramount. Also

$$g_{23} = -1 < 0$$

$$g_{11}g_{23} - g_{12}g_{13} = -4 + 5 = 1 > 0$$

i.e. condition (18) of the above Corollary is also satisfied.

Step 2. Using the algorithm in Reference 8, we find the 3-port in Figure 62 realizing the **G** matrix from Step 1.

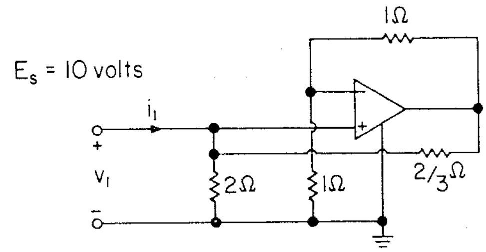


Figure 63. A circuit to realize the v–i characteristic in Figure 61

Step 3. Connecting the 3-port in Step 2 to an op amp we get the circuit in Figure 63 which realizes the characteristic shown in Figure 61.

The canonical circuit in Figure 2 is then obtained by finding the 'union' of all the circuits which realize the characteristics in Figure 1(b).

Let us now derive the slope-breakpoint inequality from Section 2. The sufficiency of these inequalities follows directly from the design formulae given in Section 2. We prove the necessity of these inequalities one case at a time. Consider the design algorithm in Figure 3(b), substituting for E_1 in R_4 we have

$$\begin{aligned}\frac{R_4}{R_3}&=\frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{E_{B2}|E_{s-}|-E_{B1}|E_{s-}|-E_{B1}^2+E_{B1}E_{B2}}\\&=\frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{|E_{s-}|(E_{B2}-E_{B1})+E_{B1}(E_{B2}-E_{B1})}\\&=\frac{(E_{B1}+|E_{s-}|)(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}{(E_{B1}+|E_{s-}|)(E_{B2}-E_{B1})}.\end{aligned} \tag{23}$$

Therefore

$$\frac{R_4}{R_3}=\frac{E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{E_{B2}-E_{B1}} \tag{24}$$

To get $R_4/R_3>0$ we need

$$\frac{E_{s+}+|E_{s-}|}{E_{B2}-E_{B1}}>1 \tag{25}$$

which is part of the slope-breakpoint inequality (1). Next, substitute for R_7 into R_6 to get

$$R_6=\frac{1+\dfrac{R_4}{R_3}}{m_1+m_0\dfrac{R_4}{R_3}} \tag{26}$$

Substituting (24) into (26) we have

$$\begin{aligned}R_6&=\frac{E_{B2}-E_{B1}+E_{s+}+|E_{s-}|+E_{B1}-E_{B2}}{m_1(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|+E_{B1}-E_{B2})}\\&=\frac{E_{s+}+|E_{s-}|}{(m_1-m_0)(E_{B2}-E_{B1})+m_0(E_{s+}+|E_{s-}|)}\end{aligned} \tag{27}$$

For R_6 to be positive the denominator in (27) must be positive, i.e.

$$(m_1-m_0)(E_{B2}-E_{B1})>-m_0(E_{s+}+|E_{s-}|)$$

or

$$\frac{m_0 - m_1}{m_0} < \frac{E_{s+} + |E_{s-}|}{E_{B2} - E_{B1}} \tag{28}$$

which is the second part of the slope-breakpoint inequality (1).

To derive the necessity of (2) consider the design algorithm of Figure 12(b). Substituting for R_4 into $R_5 + R_6$ we have

$$R_5 + R_6 = \frac{E_{s+} + |E_{s-}|}{m_0(E_{s+} + |E_{s-}|) - I_{B2} + I_{B1}} \tag{29}$$

For $R_5 + R_6$ to be positive we need the denominator in (29) to be positive, i.e.

$$m_0(E_{s+} + |E_{s-}|) > I_{B2} - I_{B1}$$

or

$$m_0 > \frac{I_{B2} - I_{B1}}{E_{s+} + |E_{s-}|} \tag{30}$$

which is condition (2) of Section 2.

Similar procedures can be used to derive these inequalities for all other cases. These are presented in Reference 14.

In summary, we would like to emphasize that the concept of a paramount matrix has been crucial in obtaining the canonical circuit of Figure 2. Indeed, each of the circuits corresponding to the characteristics in Figure 1 was obtained using our algorithm, which in step one requires the construction of an appropriate paramount matrix. Furthermore, the slope-breakpoint inequality can be shown to be an immediate conseqeunce of the paramountcy of **G**. Finally, the fact that certain characteristics cannot be realized using one opamp and positive linear resistors is again a direct consequence of the paramountcy of **G**. For example, no characteristics with $m_0 \leq 0$ can be synthesized because m_0 is the ratio of two principal minors of a paramount matrix and therefore must be strictly positive.

6. CONCLUDING REMARKS

Finally, we wish to emphasize that our *main objective* in this paper is to present a *catalogue* of designs of the class of *all* non-linear driving-point characteristics which can be realized by using only one *op amp* and *linear* positive resistors. Although many of these circuits are indeed special cases of our main canonical circuit in Figure 2, we have decided to present the individual designs in a strictly 'cook-book' style in order to encourage and facilitate wider applications of these practical op amp circuits by engineers and circuit designers not well-versed in *non-linear* circuit analysis, let alone design. Consistent with this goal, each design is supplemented by actual oscilloscope pictures because these designs are based on *d.c. analysis* and there is no guarantee that the physical circuits (especially those with negative resistance regions) will be stable in practice. In fact the robustness (relative to stability) of all circuits presented in this paper came as a pleasant surprise to us and therefore highly encouraging for future circuit designers. It should be pointed out that other negative resistance devices have also been built recently using bipolar, JFET and MOS transistors.[15,16] However, the characteristic of these circuits, although quite robust, are severely constrained by the characteristics of the transistor and can therefore only be 'massaged' slightly.[17] On the other hand, the v–i characteristics of the op-amp circuits reported in this paper can be accurately and easily adjusted to have any *prescribed* characteristic, subject only to the rather liberal inequality constraints (1) or (2). It should also be noted that an interactive software package for the design of these circuits has been developed.

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